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Examiner -- Joseph Nguyen
Applicant -- Edlin Solomon
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Application 09/871383(20020089000A1).
Art unit 2815.Mailing date 9.27.2002.

Reply №3 to Notice on 9.27.2002.

I ask to change title

BIPOLAR STATIC INDUCTION DEVICE

I forget to write on fig.5 and fig.6 simbols n, n+, p+.
n -- substrate, n+ -- sources, p+ -- gates.

I ask to cancell examination of devices without thick channels, becauce it is difficult to control them.

C1 "paragraph 0001". The invention relates to a microelectronics and more particularly to a bipolar static induction devices -- transistor and transistor-thyristor (transistor, which can be latch).

C2 "between paragraph 0001 and 0002". There exists a static induction type semiconductor device which use as a power transistor. It is of the surface gate type and is used for providing a high current density. The static induction type semiconductor device provides a plurality of a small source regions surounded by a gate region. According to this structure the channel region beneath the source region becomes small, thereby increasing the stored carrier density and enabling a large main current to flow when using a small gate current, thereby achieving a high current amplification ratio. A thin insulating film provided on the surface of the n+-source region operates as a tunnel-oxidized film, thereby enabling electrons to be injected into the source region but preventing the positive holes from being drawn out. Therefore, as the consumption of positive holes store in the channel region decreases, a sufficiently large source current is allowed to flow even if a further smaller gate current is injected, thereby further increasing the current amplification factor[1]. The drawbacks of the transistor are that it cannot operates on circuits of alternating voltage and current density is insufficient.

There exists vertical JFET, in which gate and channel are formed with implantation of impurity in doped epitaxial layer through mask - doped polysilicon drain electrode[2]. Method provides forming of the transistor with channel thickness equals about 10.sup.-7 m. The drawback of the transistor is that it cannot operates on alternating voltage circuits.

C3 "paragraph 0005". This result is achieved by disposing elements of the bipolar static induction transistor: a gate, a source, (and) a channel (as well as) and electrodes (and isolation) on each of sides of a substrate, and besides one of channels of the multielemental structure on each of sides of the substrate is thicker than other channels and it is connected to a separate electrode.

C4 "paragraph 0010". Though the structure of the transistor is symmetric the operating duty of the channel that is near the drain of the transistor essentially differs from the operating duty of the channel that is near its source. The electrical field reduces the concentration of holes in the

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TRANSMITTAL FORM

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ENCLOSURES *(check all that apply)*

- [ ] Fee Transmittal Form
  - [ ] Fee Attached
- [+] Amendment / Reply
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  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
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- [ ] After Allowance Communication to Group
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- [ ] Appeal Communication to Group (*Appeal Notice, Brief, Reply Brief*)
- [ ] Proprietary Information
- [ ] Status Letter
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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Edlin Solomon
Signature	[signature]
Date	01.23.2003

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231 on this date: 01.23.2003

Typed or printed name	Edlin Solomon		
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